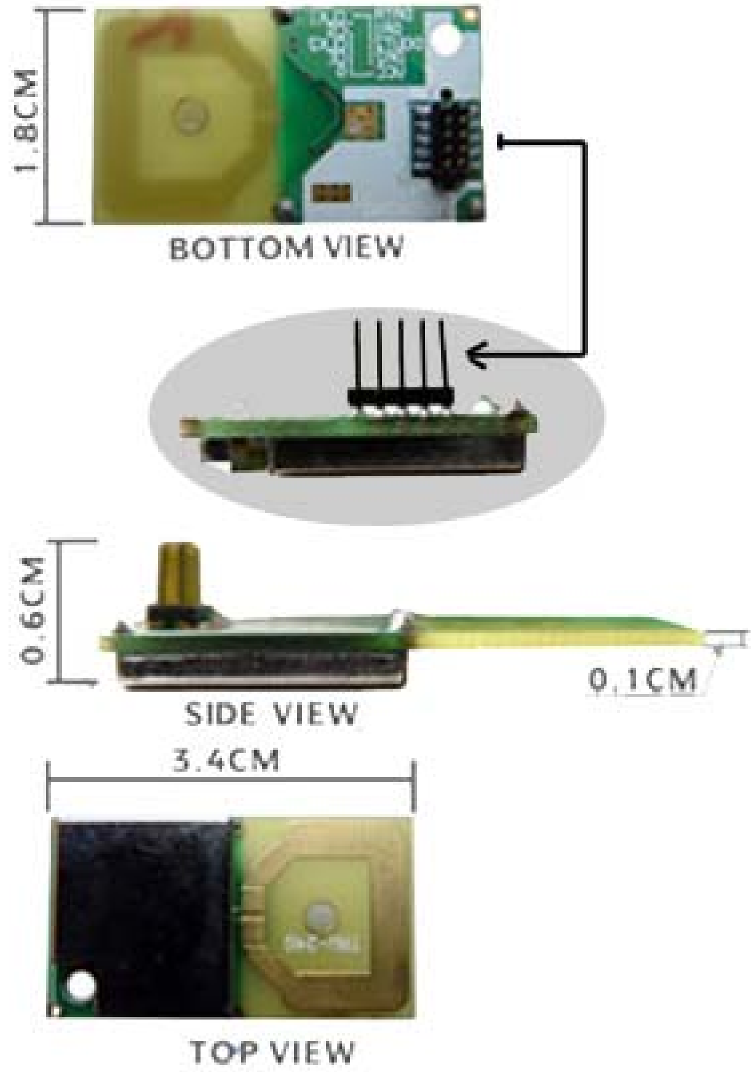
TRF-2.4G
Reference Guide

Revision 1.01 –March 2004



High frequency TRF-2.4G Transceiver module

Specification

- Frequency Range: 2.4~2.524 GHz ISM band
- Modulate Mode: GFSK
- Data Rate: 1Mbps; 250Kbps
- Multi channel operation: 125 channels, Channel switching time<200uS, Support frequency hopping
- Emulated full duplex RF link due to the 1Mbits/s on the air data rate
- Simultaneous dual receiver
- Data slicer / clock recovery of data
- Including decoder, encoder and data buffer and CRC computation
- ShockBurst mode for ultra-low power operation and relaxed MCU performance
- Sensitivity: -90dBm
- Built in antenna
- Power supply range: 1.9 to 3.6 V
- Low supply current (TX), typical 10.5mA peak@ -5dBm output power
- Low supply current (RX), typical18mA peak in receive mode
- Supply current in Power Down Mode: 1 uA
- Operating Temperature: -40~+85 Centigrade
- Size: 20.5*36.5*2.4mm
- 100% RF tested
- Competitive price

Applications

- Wireless mouse, keyboard, joystick
- Wireless data communication
- Alarm and security systems
- Home automation
- Wireless Earphone
- Telemetry
- Surveillance
- Automotive

GENERAL DESCRIPTION

Laipac TRF-2.4G Module is an easy to use radio transceiver for the world wide 2.4 - 2.5 GHz ISM band. The transceiver consists of an antenna, a fully integrated frequency synthesizer, a power amplifier, a crystal oscillator and a modulator. Output power and frequency channels are easily programmable by use of the 3-wire serial interface. Current consumption is very low, only 10.5mA at an output power of -5dBm and 18mA in receive mode. Built-in Power Down modes makes power saving easily realizable.

ELECTRICAL SPECIFICATIONS

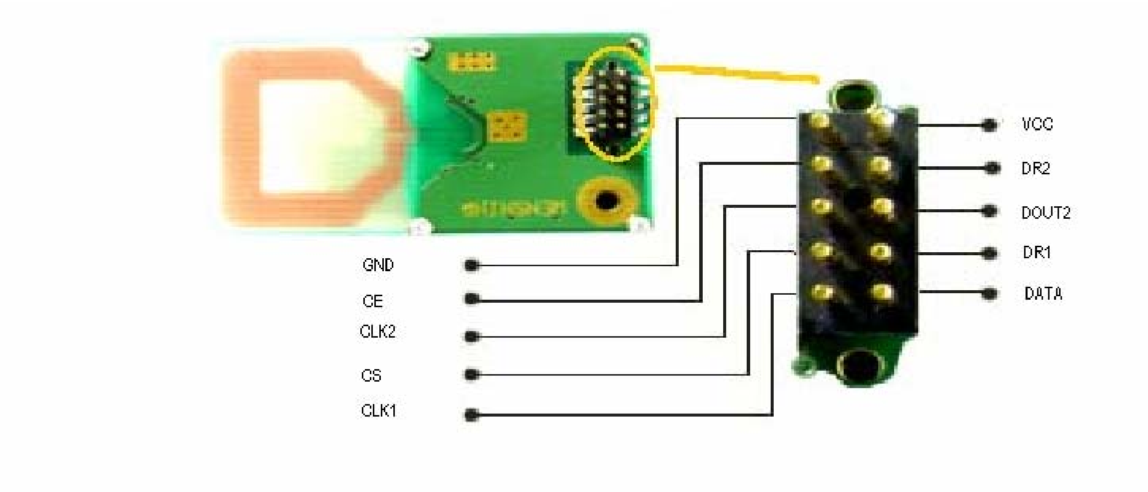
Conditions: VCC = +3V, VSS = 0V, TA = - 40ºC to + 85ºC

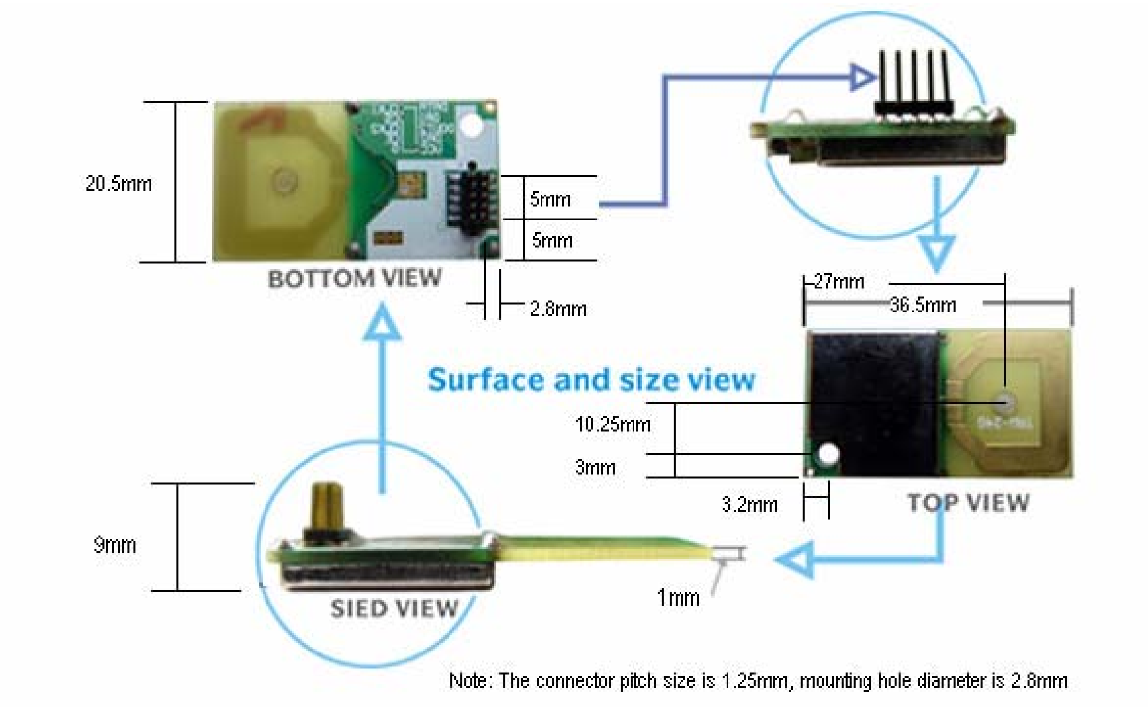
Symbol	Parameter (condition)	Notes	Min.	Ttp.	Max.	Units
	Operating conditions					
VCC	Supply voltage		1.9	3.0	3.6	V
TEMP	Operating Temperature		-40	+27	+85	ºC
	Digital input pin					
V_{IH}	HIGH level input voltage		VCC-0.3		VCC	V
V_{IL}	LOW level input voltage		Vss		0.3	V
	Digital output pin					
V_{OH}	HIGH level output voltage (IOH=-0.5mA)		VCC-0.3		VCC	V
V_{OL}	LOW level output voltage (IOL=0.5mA)		Vss		0.3	V
	General RF conditions					
f_{OP}	Operating frequency	1)	2400		2524	MHz
□f	Frequency deviation			±156		kHz
R_{GFSK}	Data rate ShockBurst		>0		1000	kbps
R_{GFSK}	Data rate Direct Mode	2)	250		1000	kbps
$F_{CHANNEL}$	Channel spacing			1		MHz
	Transmitter operation					
P_{RF}	Maximum Output Power	3)		0	+4	dBm
P_{RFC}	RF Power Control Range		16	20		dB
P_{RFCR}	RF Power Control Range Resolution				±3	dB
P_{BW}	20dB Bandwidth for Modulated Carrier				1000	kHz
P_{RF2}	2nd Adjacent Channel Transmit Power 2MHz				-20	dBm
P_{RF3}	3rd Adjacent Channel Transmit Power 3MHz				-40	dBm
I_{VCC}	Supply current @ 0dBm output power	4)		13		mA
I_{VCC}	Supply current @ -20dBm output power	4)		8.8		mA
I_{VCC}	Average Supply current @ -5dBm output power, ShockBurst	5)		0.8		mA
I_{VCC}	Average Supply current in stand-by mode	6)		12		□A
I_{VCC}	Average Supply current in power down			1		□A
	Receiver operation					
I_{VCC}	Supply current one channel 250kbps			18		mA
I_{VCC}	Supply current one channel 1000kbps			19		mA
I_{VCC}	Supply current two channels 250kbps			23		mA
I_{VCC}	Supply current two channels 1000kbps			25		mA
RX_{SENS}	Sensitivity at 0.1%BER (@250kbps)			-90		dBm
RX_{SENS}	Sensitivity at 0.1%BER (@1000kbps)			-80		dBm
C/I_{CO}	C/I Co-channel			6		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 1MHz			-1		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 2MHz			-16		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 3MHz			-26		dB
RX_B	Blocking Data Channel 2			-41		dB

1) Usable band is determined by local regulations
2) Data rate must be either 250kbps or 1000kbps.
3) De-embedded Antenna load impedance = 400 □
4) De-embedded Antenna load impedance = 400 □. Effective data rate 250kbps or 1Mbps.
5) De-embedded Antenna load impedance = 400 □. Effective data rate 10kbps.
6) Current if 4 MHz crystal is used.

Table 1 TRF-2.4G RF specifications

PIN ASSIGNMENT





PIN FUNCTIONS

Pin	Name	Pin funtion	Description
1	GND	Power	Gound (0V)
2	CE	Input	Chip Enable activates RX or TX mode
3	CLK2	I/O	Clock outpu/input for RX data channel 2
4	CS	Input	Chip Select activates Configuration mode
5	CLK1	I/O	Clock Input(TX)&I/O(RX) for data channel 1 3-wire interface
6	DATA	I/O	RX data channel 1/TX data input /3-wire interface
7	DR1	Output	RX data ready at data channel 1 (ShockBurst only)
8	DOUT2	Output	RX data channel 2
9	DR2	Output	RX data ready at data channel 2 (ShockBurst only)
10	VCC	Power	Power Supply (+3V DC)

Table 2 TRF-2.4G pin function

MODE OF OPERATION

TRF-2.4G can be set in the following main mode:

Mode	CE	CS
Active (RX /TX)	1	0
Configuration	0	1
Stand by	0	0

Table 3 TRF-2.4G main modes

TRF-2.4G has two active (RX /TX) modes:

- ShockBurst
- Direct Mode

The device functionality in these modes is decided by the content of a configuration word. This configuration word is presented in configuration section.

Absolute Maximum Ratings

Supply voltages

VCC............................- 0.3V to + 3.6V

VSS 0V

Input/Output voltages

V_I ....- 0.3V to VCC + 0.3V

V_O ....- 0.3V to VCC + 0.3V

Total Power Dissipation

P_D (T_A=85□C)..............................90mW

Temperatures

Operating Temperature…. - 40□C to + 85□C

Storage Temperature……. - 40□C to + 125□C

ShockBurst Mode

The ShockBurst technology uses on-chip FIFO to clock in data at a low data rate
and transmit at a very high rate thus enabling extremely power reduction.
When operating the TRF-2.4G in ShockBurst, you gain access to the high data rates (1 Mbps) offered by the 2.4 GHz band without the need of a costly, high-speed micro
controller (MCU) for data processing.
By putting all high speed signal processing related to RF protocol on-chip, the TRF-2.4G offers the following benefits:

- □Highly reduced current consumption
- □Lower system cost (facilitates use of less expensive micro controller)
- □Greatly reduced risk of 'on-air' collisions due to short transmission time

The TRF-2.4G can be programmed using a simple 3-wire interface where the data rate is decided by the speed of the micro controller.
By allowing the digital part of the application to run at low speed while maximizing
the data rate on the RF link, the nRF ShockBurst mode reduces the average current consumption in applications considerably.

ShockBurst principle

When the TRF-2.4G is configured in ShockBurst, TX or RX operation is conducted in the following way (10 kbps for the example only).

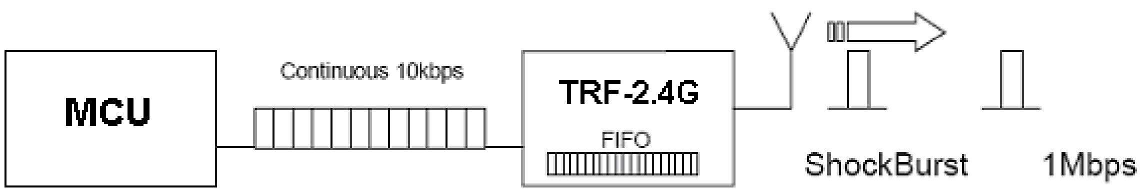


Figure 0 Clocking in data with MCU and sending with ShockBursttechnology

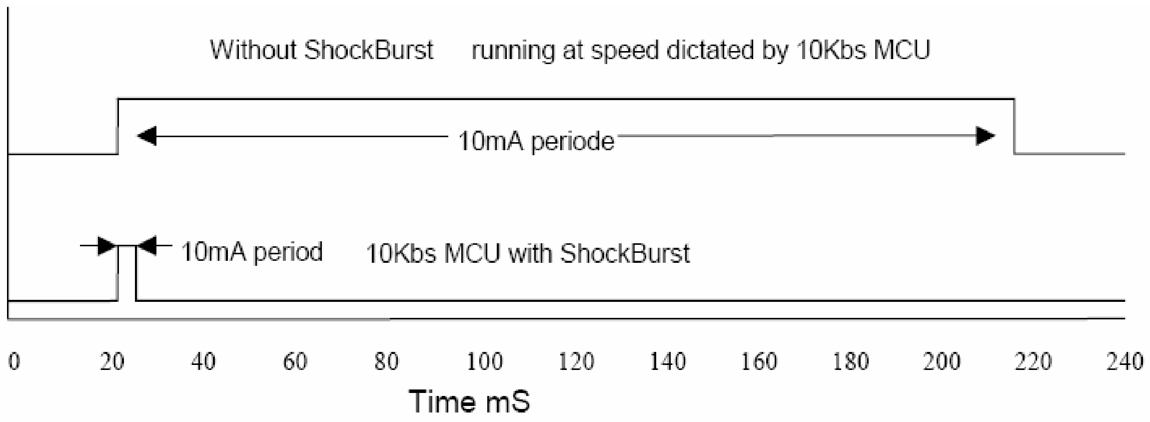


Figure 1 Current consumption with & without ShockBurst technology

TRF-2.4G ShockBurst Transmit:

MCU interface pins: CE, CLK1, DATA

1. When the application MCU has data to send, set CE high. This activates TRF-2.4G on-board data processing.
2. The address of the receiving node (RX address) and payload data is clocked into the TRF-2.4G. The application protocol or MCU sets the speed <1Mbps (ex: 10kbps).
3. MCU sets CE low, this activates a TRF-2.4G ShockBurst transmission.
4. TRF-2.4G ShockBurst:
    1. RF front end is powered up
    2. RF package is completed (preamble added, CRC calculated)
    3. Data is transmitted at high speed (250 kbps or 1 Mbps configured by user).
    4. TRF-2.4G return to stand-by when finished

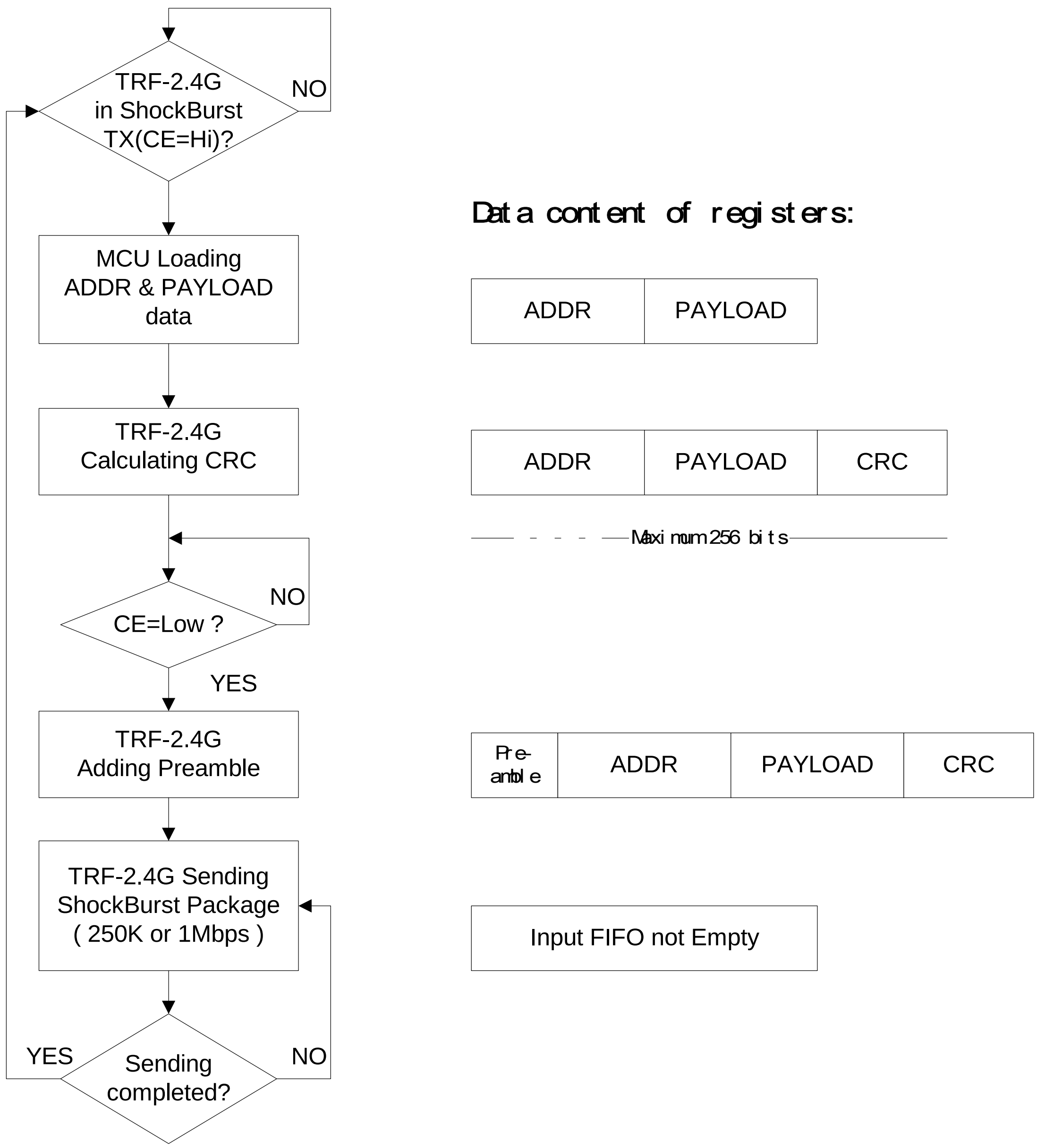


Figure 2 Flow Chart ShockBurst Transmit of TRF-2.4G

TRF-2.4G ShockBurst Receive:

MCU interface pins: CE, DR1, CLK1 and DATA (one RX channel receive)

1. Correct address and size of payload of incoming RF packages are set when TRF-2.4G is configured to ShockBurst RX.
2. To activate RX, set CE high.
3. After 200 □s settling, TRF-2.4G is monitoring the air for incoming communication.
4. When a valid package has been received (correct address and CRC found), TRF-2.4G removes the preamble, address and CRC bits.
5. TRF-2.4G then notifies (interrupts) the MCU by setting the DR1 pin high.
6. MCU may (or may not) set the CE low to disable the RF front end (low current mode).
7. The MCU will clock out just the payload data at a suitable rate (ex. 10 kbps).
8. When all payload data is retrieved TRF-2.4G sets DR1 low again, and is ready for new incoming data package if CE is kept high during data download. If the CE was set low, a new start up sequence can begin, see Figure 2.

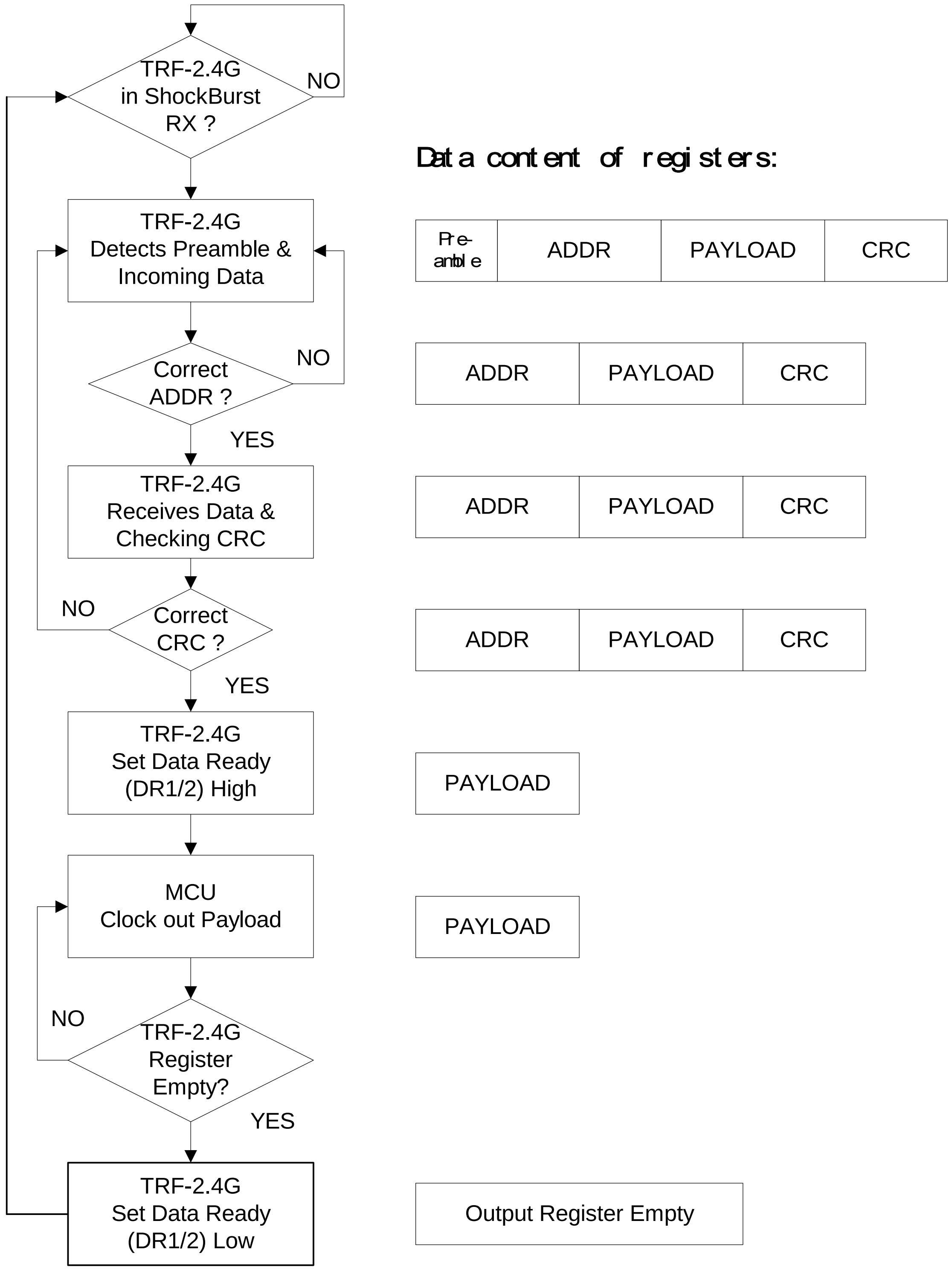


Figure 3 Flow Chart ShockBurst Receive of TRF-2.4G

TRF-2.4G Direct Mode:

In direct mode the TRF-2.4G works like a traditional RF device. Data must be at 1Mbps, or 250kbps at low data rate setting, for the receiver to detect the signals.

Direct Mode Transmit:

MCU interface pins: CE, DATA

1. When application MCU has data to send, set CE high
2. The TRF-2.4G RF front end is now immediately activated, and after 200 seconds settling time, data will modulate the carrier directly.
3. All RF protocol parts must hence be implemented in MCU firmware (preamble, address and CRC).

Direct Mode Receive:

MCU interface pins: CE, CLK1, and DATA

1. Once the TRF-2.4G is configured and powered up (CE high) in direct RX mode, DATA will start to toggle due to noise present on the air.
2. CLK1 will also start to toggle as TRF-2.4G is trying to lock on to the incoming data stream.
3. Once a valid preamble arrives, CLK1 and DATA will lock on to the incoming signal and the RF package will appear at the DATA pin with the same speed as it is transmitted.
4. To enable the demodulator to re-generate the clock, the preamble must be 8 bits toggling hi-low, starting with low if the first data bit low.
5. In this mode no data ready (DR) signals is available. Address and checksum verification must also be done in the receiving MC.

DuoCeiver Simultaneous Two Channel Receive Mode

In both ShockBurst & Direct modes the TRF-2.4G can facilitate simultaneous reception of two parallel independent frequency channels at the maximum data rate.

This means:

1. TRF-2.4G can receive data from two 1 Mbps transmitters, 8 MHz (8 frequency channels) apart through one antenna interface.
2. The output from the two data channels is fed to two separate MCU interfaces.
3. Data channel 1: CLK1, DATA, and DR1
4. Data channel 2: CLK2, DOUT2, and DR2
5. DR1 and DR2 are available only in ShockBurst.

The DuoCeiver technology provides 2 separate dedicated data channels for RX and replaces the need for two, stand alone receiver systems.

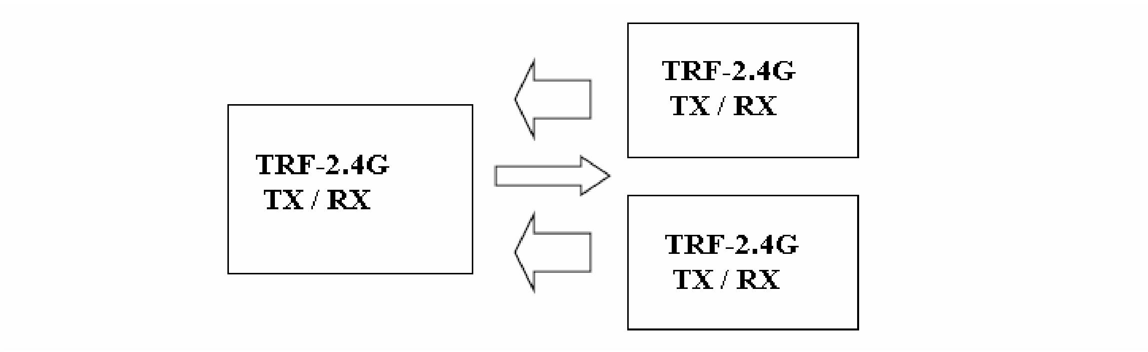
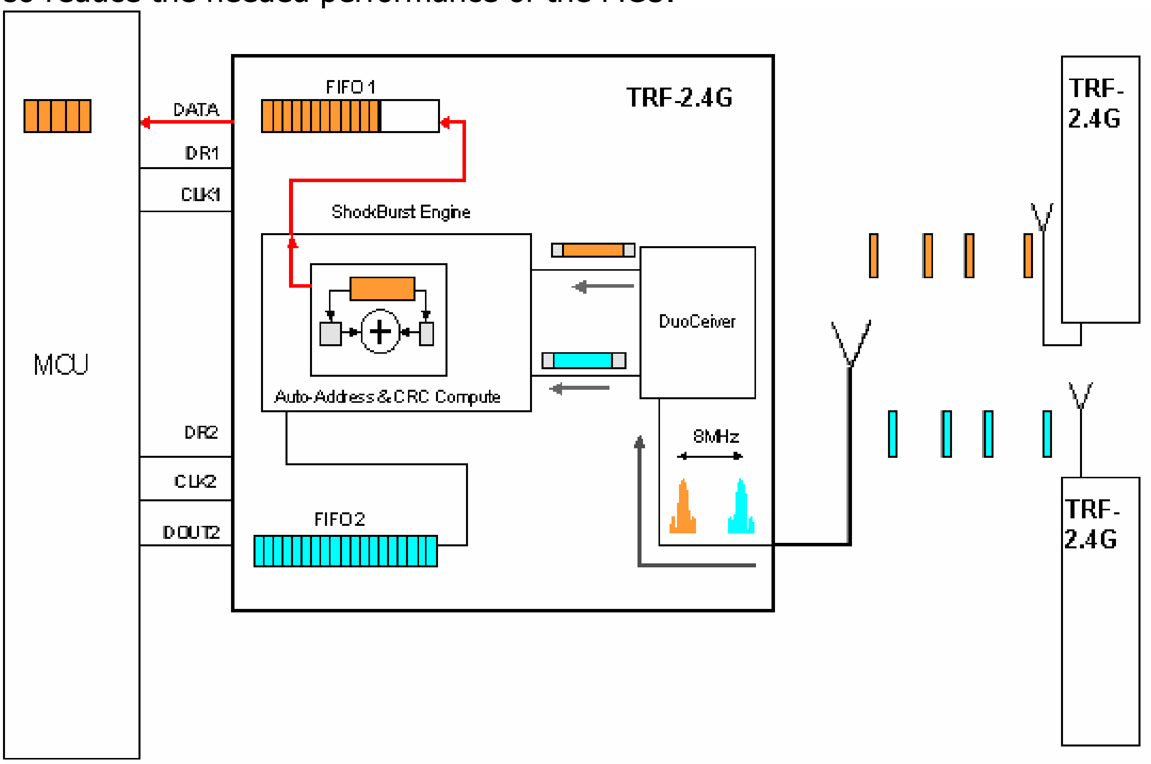


Figure 4 Simultaneous 2 channel receive on TRF-2.4G

There is one absolute requirement for using the second data channel. For the TRF-2.4G to be able to receive at the second data channel the frequency channel must be 8MHz higher than the frequency of data channel 1. The TRF-2.4G must be programmed to receive at the frequency of data channel 1. No time ultiplexing is used in TRF-2.4G to fulfil this function. In direct mode the MCU must be able to handle two simultaneously incoming data packets if it is not multiplexing between the two data channels. In ShockBurst it is possible for the MCU to clock out one data channel at a time while data on the other data channel waits for MCU availability, without any lost data packets, and by doing so reduce the needed performance of the MCU.



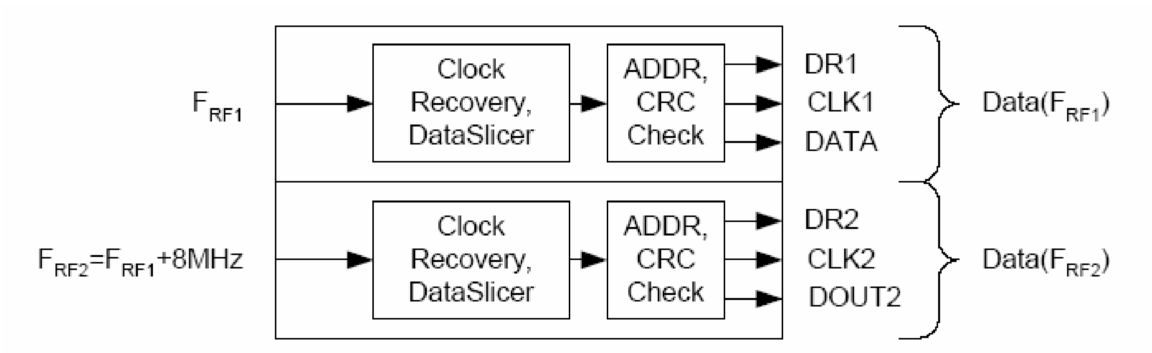


Figure 5 DuoCeiver with two simultaneously independent receive channels.

Configuration Mode

In configuration mode a configuration word of up to 15 bytes is downloaded to TRF-2.4G. This is done through a simple 3-wire interface (CS, CLK1 and DATA). For more information on configuration please refer to the TRF-2.4G Device configuration chapter on next 2nd page.

Stand-By Mode

Stand by mode is used to minimize average current consumption while maintaining short start up times. In this mode, part of the crystal oscillator is active. Current consumption is dependent on crystal frequency (Ex: 12uA @ 4 MHz, 32uA@ 16MHz). The configuration word content is maintained during stand by.

Power Down Mode

In power down the TRF-2.4G is disabled with minimal current consumption, typically less than 1□A. Entering this mode when the device is not active minimizes average current consumption, maximizing battery lifetime. The configuration word content is maintained during power down.

DEVICE CONFIGURATION

All configuration of the TRF-2.4G is done via a 3-wire interface to a single configuration register. The configuration word can be up to 15 bytes long for ShockBurst use and up to 2 bytes long for direct mode.

Configuration for ShockBurst operation

The configuration word in ShockBurst enables the TRF-2.4G to handle the RF protocol. Once the protocol is completed and loaded into TRF-2.4G only one byte,
bit[7:0], needs to be updated during actual operation.

The configuration blocks dedicated to ShockBurst is as follows:

Payload section width: Specifies the number of payload bits in a RF package. This enables the TRF-2.4G to distinguish between payload data and the CRC bytes in a received package.

Address width: Sets the number of bits used for address in the RF package. This enables the TRF-2.4G to distinguish between address and payload data.

Address (RX Channel 1 and 2): Destination address for received data.

CRC: Enables TRF-2.4G on-chip CRC generation and de-coding.

NOTE:
These configuration blocks, with the exception of the CRC, are dedicated for the packages that a TRF-2.4G is to receive.
In TX mode, the MCU must generate an address and a payload section that fits the configuration of the TRF-2.4G that is to receive the data.
When using the TRF-2.4G on-chip CRC feature ensure that CRC is enabled and uses the same length for both the TX and RX devices.

PRE-AMBLE	ADDRESS	PAYLOAD	CRC

Figure 6 Data packet set-up

Configuration for Direct Mode operation

For direct mode operation only the two first bytes (bit[15:0]) of the configuring word are relevant.

Configuration Word overview

	Bit position	Number of bits	Name	Function
ShockBurst configuration	143:120	24	TEST	Reserved for testing
	119:112	8	DATA2_W	Length of data payload section RX channel 1
	111:104	8	DATA1_W	Length of data payload section RX channel 1
	103:64	40	ADDR2	Up to 5 bytes address for channel 2
	63:24	40	ADDR1	Up to 5 bytes address for channel 1
	23:18	6	ADDR_W	Number of address bits(both RX channels)
	17	1	CRC_L	8 or 16 bits CRC
	16	1	CRC_EN	Enable on-chip CRC generation/checking
General device configuration	15	1	RX2_EN	Enable two channel receive mode
	14	1	CM	Communication mode (Direct or ShockBurst)
	13	1	RFDR_SB	RF data rate (1Mbps requires 16MHz crystal)
	12:10	3	XO_F	Crystal frequency (Factory default 16MHz crystal mounted)
	9:8	2	RF_PWR	RF output power
	7:1	7	RF_CH#	Frequency channel
	0	1	RXEN	RX or TX operation

Table 4 Table of configuration words.

The configuration word is shifted in MSB first on positive CLK1 edges. New configuration is enabled on the falling edge of CS.

NOTE.
On the falling edge of CS, the TRF-2.4G updates the number of bits actually shifted in during the last configuration.
Ex:
If the TRF-2.4G is to be configured for 2 channel RX in ShockBurst, a total of 120 bits must be shifted in during the first configuration after VCC is applied.
Once the wanted protocol, modus and RF channel are set, only one bit (RXEN) is shifted in to switch between RX and TX.

Configuration Word Detailed Description

The following describes the function of the 144 bits (bit 143 = MSB) that is used to configure the TRF-2.4G.

General Device Configuration: bit[15:0]
ShockBurst Configuration: bit[119:0]
Test Configuration: bit[143:120]

MSB	TEST							
D143	D142	D141	D140	D139	D138	D137	D136	
Reserved for testing								
1	0	0	0	1	1	1	0	Default

MSB	TEST															
D135	D134	D133	D132	D131	D130	D129	D128	D127	D126	D125	D124	D123	D122	D121	D120	
Reserved for testing														Close PLL in TX		
0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0	Default

DATA2_W								
D119	D118	D117	D116	D115	D114	D113	D112	
Data width channel#2 in # of bits excluding addr/crc								
0	0	1	0	0	0	0	0	Default

DATA1_W								
D111	D110	D109	D108	D107	D106	D105	D104	
Data width channel#1 in # of bits excluding addr/crc								
0	0	1	0	0	0	0	0	Default

ADDR2												
D103	D102	D101	….	D71	D70	D69	D68	D67	D66	D65	D64	
Channel#2 Address RX (up to 40bit)												
0	0	0	…	1	1	1	0	0	1	1	1	Default

ADDR1												
D63	D62	D61	….	D31	D30	D29	D28	D27	D26	D25	D24	
Channel#1 Address RX (up to 40bit)												
0	0	0	…	1	1	1	0	0	1	1	1	Default

ADDR_W						
D23	D22	D21	D20	D19	D18	
Address width in # of bits (both channels)						
0	0	1	0	0	0	Default

CRC		
D17	D16	
CRC Mode 1 = 16bit, 0 = 8bit	CRC 1 = enable; 0 = disable	
0	1	Default

RF-Programming															LSB	
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Two Ch.	BUF	OD	XO Frequency			RF Power		Channel selection							RXEN	
0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0	Default

Table 5 Configuration data word

The MSB bit should be loaded first into the configuration register.

ShochBurst configuation:

The section B[119:16] contains the segments of the configuration register dedicated to ShockBurst operational protocol. After VCC is turned on ShockBurst configuration is done once and remains set whilst VCC is present. During operation only the first byte for frequency channel and RX/TX switching need to be changed.

DATAx_W

DATA2_W							
119	118	117	116	115	114	113	112

DATA1_W							
111	110	109	108	107	106	105	104

Table 6 Number of bits in payload.

Bit 119 – 112:
DATA2_W: Length of RF package payload section for receive-channel 2.
Bit 111 – 104:
DATA1_W: Length of RF package payload section for receive-channel 1.
NOTE:
The total number of bits in a ShockBurst RF package may not exceed 256!
Maximum length of payload section is hence given by:
DATAx_W(bits) = 256-ADDR_W - CRC
Where:
ADDR_W: length of RX address set in configuration word B[23:18]
CRC: check sum, 8 or 16 bits set in configuration word B[17]
PRE: preamble, 4 or 8 bits are automatically included
Shorter address and CRC leaves more room for payload data in each package.

ADDRx

ADDR2											
103	102	101	… …	71	70	69	68	67	66	65	64

ADDR1											
63	62	61	… …	31	30	29	28	27	26	25	24

Table 7 Address of receiver #2 and receiver #1.

Bit 103 – 64:
ADDR2: Receiver address channel 2, up to 40 bit.
Bit 63 – 24: ADDR1
ADDR1: Receiver address channel 1, up to 40 bit.
NOTE!
Bits in ADDRx exceeding the address width set in ADDR_W are redundant
and can be set to logic 0.

ADDR_W& CRC

ADDR_W						CRC_L	CRC_EN
23	22	21	20	19	18	17	16

Table 8 Number of bits reserved for RX address + CRC setting.

Bit 23 – 18:
ADDR_W: Number of bits reserved for RX address in ShockBurst packages.
NOTE:
Maximum number of address bits is 40 (5 bytes). Values over 40 in ADDR_W are not valid.
Bit 17:
CRC_L: CRC length to be calculated by TRF-2.4G in ShockBurst.
Logic 0: 8 bit CRC
Logic 1: 16 bit CRC
Bit: 16:
CRC_EN: Enables on-chip CRC generation (TX) and verification (RX).
Logic 0: On-chip CRC generation/checking disabled
Logic 1: On-chip CRC generation/checking enabled
NOTE:
An 8 bit CRC will increase the number of payload bits possible in each ShockBurst data packet, but will also reduce the system integrity.

General device configuration:

This section of the configuration word handles RF and device related parameters.
Modes:

RX2_EN	CM	RFDR_SB	XO_F			RF_PWR	
15	14	13	12	11	10	9	8

Table 9 RF operational settings.

Bit 15:
RX2_EN:
Logic 0: One channel receive
Logic 1: Two channels receive
NOTE:
In two channels receive, the TRF-2.4G receives on two, separate frequency channels simultaneously. The frequency of receive channel 1 is set in the configuration word B[7-1], receive channel 2 is always 8 channels (8 MHz) above receive channel 1.
Bit 14:
Communication Mode:
Logic 0: TRF-2.4G operates in direct mode.
Logic 1: TRF-2.4G operates in ShockBurst mode
Bit 13:
RF Data Rate:
Logic 0: 250 kbps
Logic 1: 1 Mbps
NOTE:
Utilizing 250 kbps instead of 1Mbps will improve the receiver

sensitivity by 10 dB. 1Mbps requires 16MHz crystal.

Bit 12-10:

XO_F: Selects the TRF-2.4G crystal frequency to be used:

XO FREQUENCY SELECTION			
D12	D11	D10	Crystal Frequency (MHz)
0	1	1	16
Factory default: 16MHz Crystal is used inside module			

Table 10 Crystal frequency setting.

Bit 9-8:

RF_PWR: Sets TRF-2.4G RF output power in transmit mode:

RF OUTPUT POWER		
D9	D8	P (dBm)
0	0	-20
0	1	-10
1	0	-5
1	1	0

Table 11 RF output power setting.

RF channel & direction

RF_CH#							RXEN
7	6	5	4	3	2	1	0

Table 12 Frequency channel + RX / TX setting.

Bit 7 – 1:

RF_CH#: Sets the frequency channel the TRF-2.4G operates on.

The channel frequency in ***transmit*** is given by:

$Channel_{RF}$ *= 2400MHz + RF_CH# *1.0MHz*

RF_CH #: between 2400MHz and 2527MHz may be set.

The channel frequency in ***data channel 1*** is given by:

$Channel_{RF}$ *= 2400MHz + RF_CH# *1.0MHz (Reiceive at PIN#8)*

RF_CH #: between 2400MHz and 2524MHz may be set.

NOTE:

The channels above 83 can only be utilized in certain territories (ex: Japan)

The channel frequency in ***data channel 2*** is given by:

$Channel_{RF}$ *= 2400MHz + RF_CH# *1.0MHz+8MHz (Reiceive at PIN#4) ???*

RF_CH #: between 2408MHz and 2524MHz may be set.

Bit 0:

Set active mode:

Logic 0: transmit mode

Logic 1: receive mode

DATA PACKAGE DESCRIPTION

PRE-AMBLE	ADDRESS	PAYLOAD	CRC

Figure 7 Data Package Diagram

The data packet for both ShockBurst mode and direct mode communication is divided into 4 sections. These are:

1 PREAMBLE	☐The preamble field is required in ShockBurst and Direct modes ☐Preamble is 8 (or 4) bits in length and is dependent of the first data bit in direct mode. PREAMBLE 1st ADDR-BIT 01010101 0 10101010 1 ☐Preamble is automatically added to the data packet in ShockBurst and thereby gives extra space for payload. ☐In ShockBurst mode the preamble is stripped from the received output data, in direct mode the preamble is transparent to the output data.
2 ADDRESS	☐The address field is required in ShockBurst mode. ☐8 to 40 bits length. ☐Address automatically removed from received packet in ShockBurst mode. In Direct mode MCU must handle address.
3 PAYLOAD	☐The data to be transmitted ☐In Shock-Burst mode payload size is 256 bits minus the following: (Address: 8 to 40 bits. + CRC 8 or 16 bits). ☐In Direct mode the payload size is defined by 1Mbps for 4ms: 4000 bits minus the following: (Preamble: 8 (or 4) bits. + Address: 8 to 40 bits. + CRC: 0, 8 or 16 bits).
4 CRC	☐The CRC is optional in ShockBurst mode, and is not used in Direct mode. ☐8 or 16 bits length ☐The CRC is stripped from the received output data.

Table 13 Data package description

IMPORTANT TIMING DATA

The following timing applies for operation of TRF-2.4G.

TRF-2.4G Timing Information

TRF-2.4G timing	Max.	Min.	Name
PWR_DWN => ST_BY mode	3ms		Tpd2sby
PWR_DWN =>Active mode (RX/TX)	3ms		Tpd2a
ST_BY => TX ShockBurst	195□s		Tsby2txSB
ST_BY => TX Direct Mode	202□s		Tsby2txDM
ST_BY => RX mode	202□s		Tsby2rx
Minimum delay from CS to data		5□s	Tcs2data
Minimum delay from CE to data		5□s	Tce2data
Minimum delay from DR1/2 to clk		50ns	Tdr2clk
Maximum delay from clk to data	50ns		Tclk2data
Delay between edges		50ns	Td
Setup time		500ns	Ts
Hold time		500ns	Th
Delay to finish internal GFSK data		1/data rate	Tfd
Minimum input clock high		500ns	Thmin
Set-up of data in Direct Mode	50ns		Tsdm
Minimum clock high in Direct Mode		300ns	Thdm
Minimum clock low in Direct Mode		230ns	Tldm

Table 14 Switching times for TRF-2.4G

When the TRF-2.4G is in power down it must always settle in stand-by (Tpd2sby) before it can enter configuration or one of the active modes.

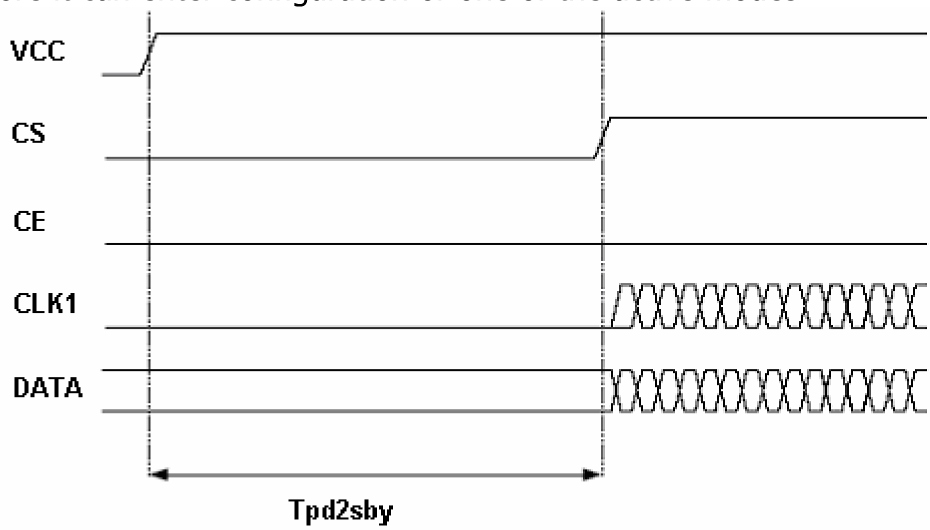


Figure 8 Timing diagram for power down (or VCC off) to stand by mode

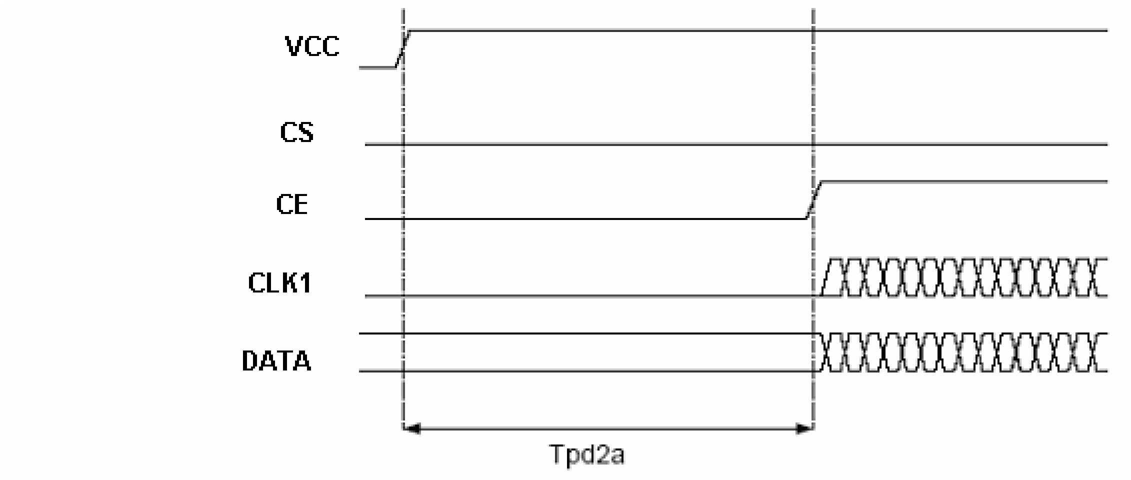


Figure 9 Power down (or VCC off) to active mode

Note that the configuration word will be lost when VCC is turned off and that the device then must be configured before going to one of the active modes. If the device is configured one can go directly from power down to the wanted active mode.

Note:

CE and CS may not be high at the same time. Setting one or the other decides whether configuration or active mode is entered.

Configuration mode timing

When one or more of the bits in the configuration word needs to be changed the following timing apply.

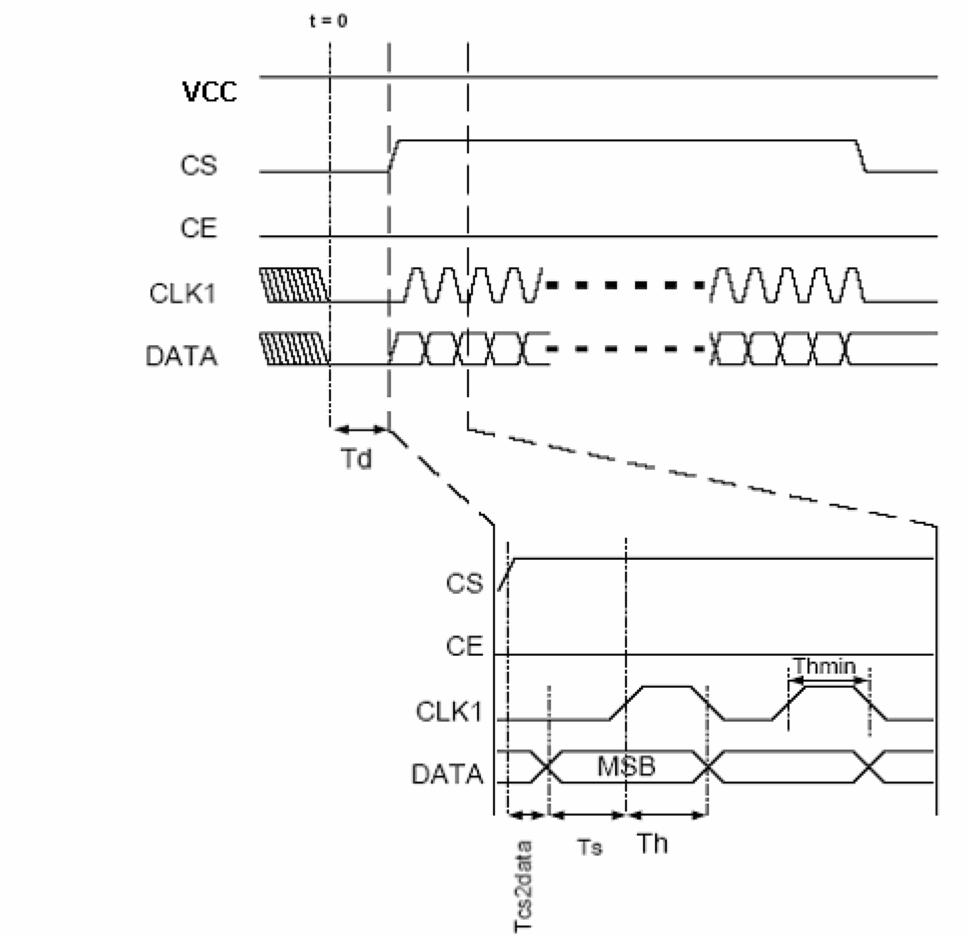


Figure 10 Timing diagram for configuration of TRF-2.4G

If configuration mode is entered from power down, CS can be set high after Tpd2sby as shown in Figure 10.

ShockBurst mode timing

ShockBurst TX:

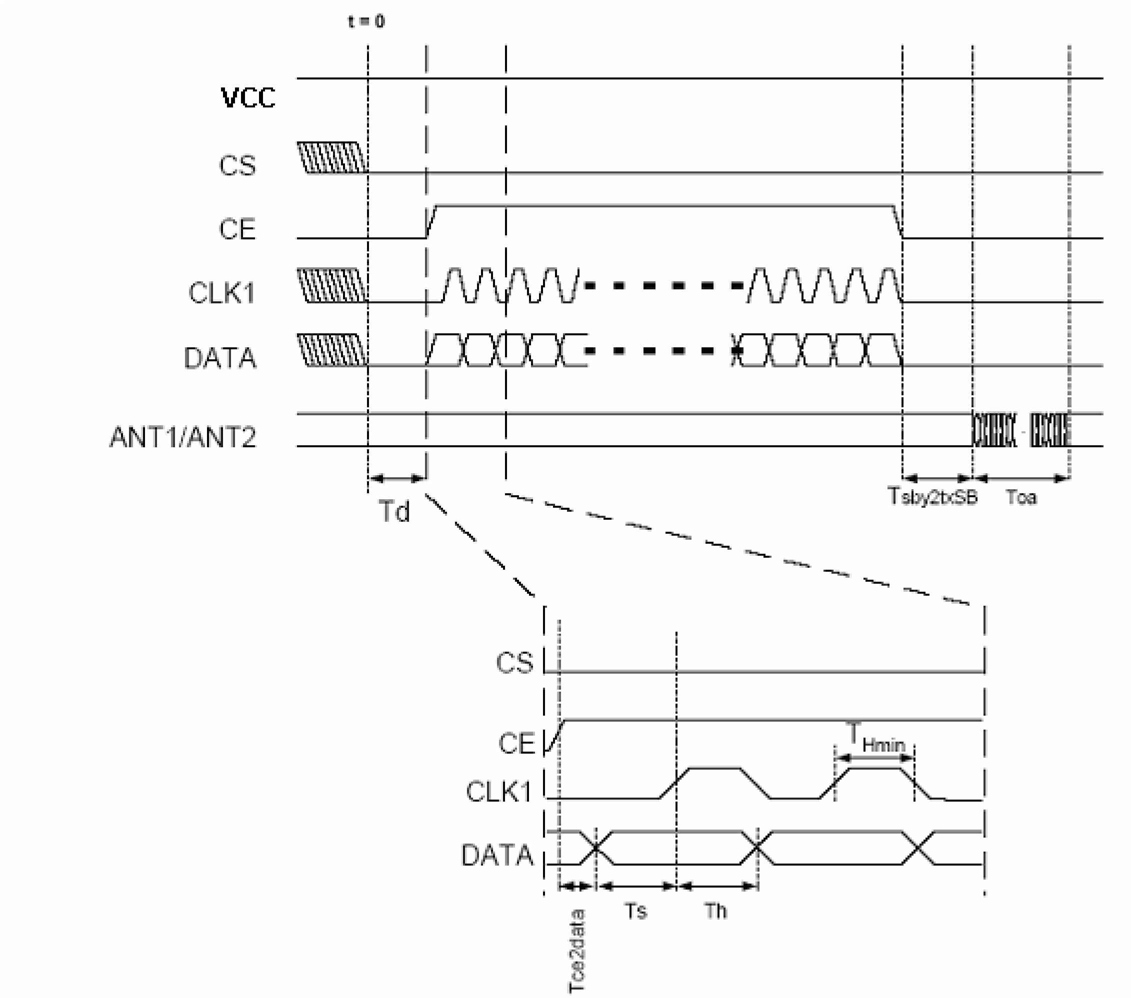


Figure 11 Timing of ShockBurst in TX

The package length and the data rate give the delay Toa (time on air), as shown in the equation.

$$T_{OA} = 1/datarate * (\#databits + 1)$$

ShockBurst RX:

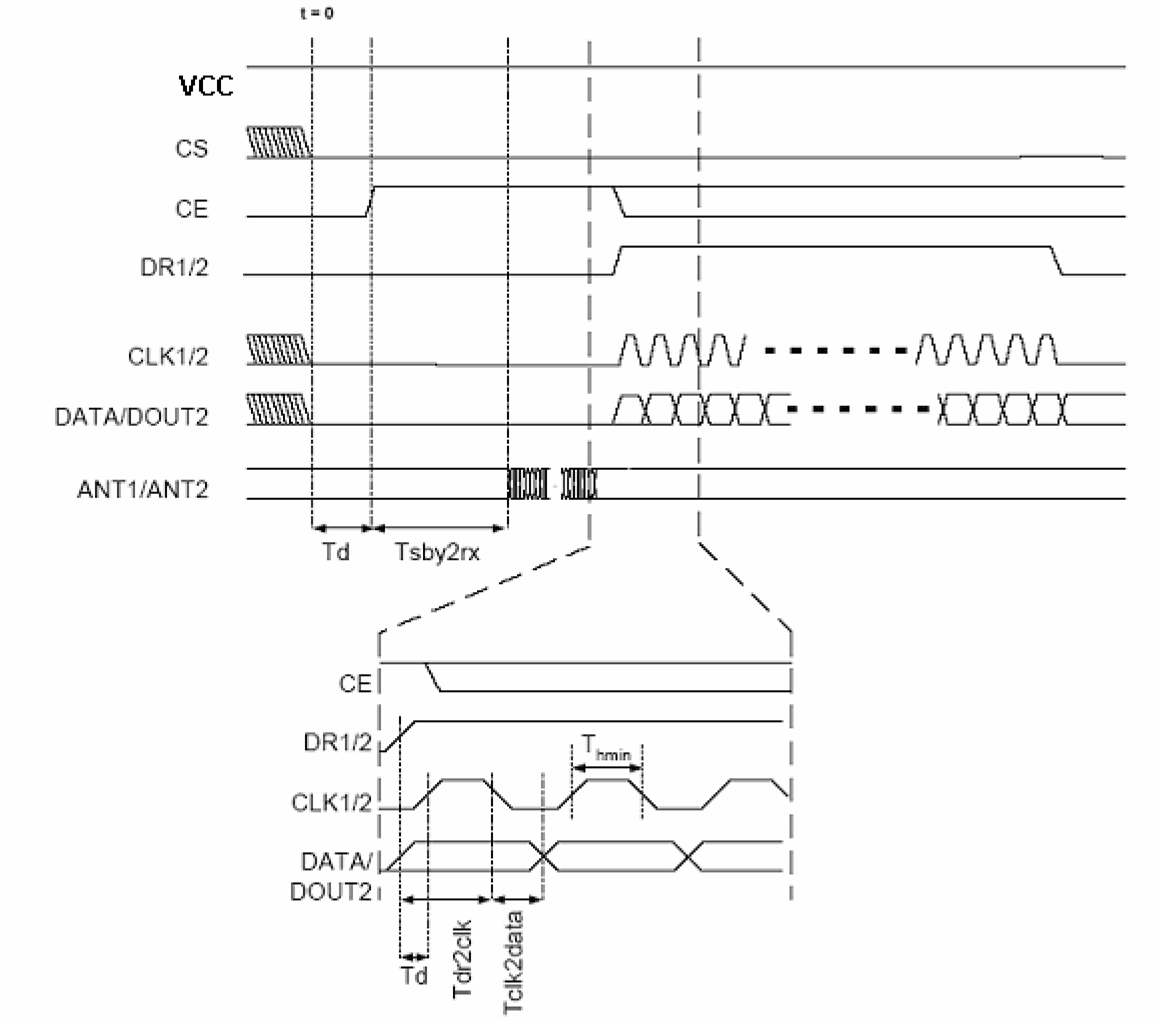


Figure 12 Timing of ShockBurst in RX

The CE may be kept high during downloading of data, but the cost is higher current consumption (18mA) and the benefit is no start-up time (200□s) after the DR1 goes low.

Direct Mode

Direct Mode TX

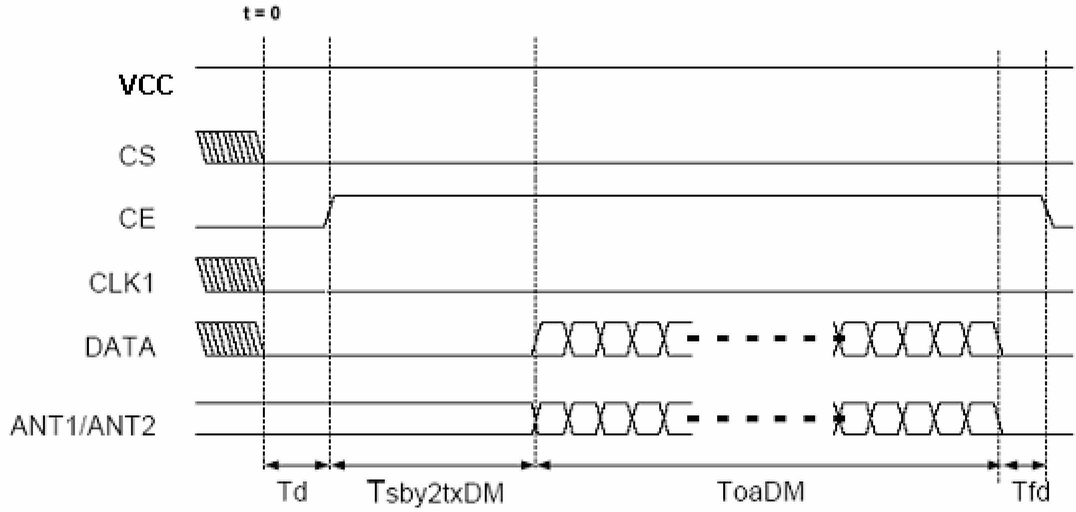


Figure 13 Timing of direct mode TX

In TX direct mode the input data will be sampled by TRF-2.4G and therefore no clock is needed. The clock must be stable at low level during transmission due to noise considerations. The exact delay Tsby2txDM is given by the equation:

$$T_{sby2txDM} = 194uS + 1/F_{XO} * 14 + 2.25uS$$

Direct Mode RX

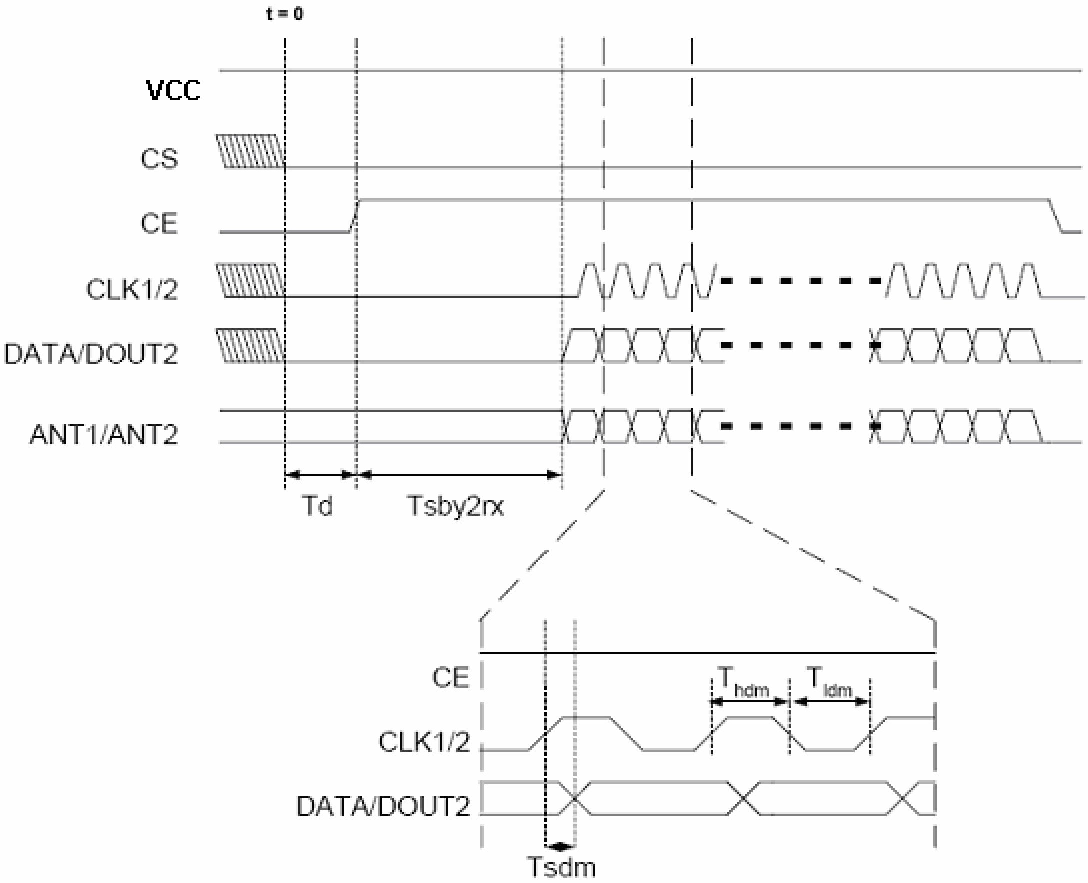


Figure 14 Timing of direct mode RX

Tsby2rx describes the delay from the positive edge of CE to the start detection of (demodulated) incoming data.

PERIPHERAL RFINFORMATION

Antenna output

The ANT1 & ANT2 output pins provide a balanced RF output to the antenna. The pins must have a DC path to VCC, either via a RF choke or via the center point in a dipole antenna. The load impedance seen between the ANT1/ANT2 outputs should be in the range 200-700 ohm. A de-embedded load impedance i.e. impedance seen at drain terminals of the output transistors of 400 ohm is recommended for maximum output power (0dBm). Lower load impedance (for instance 50 ohm) can be obtained by fitting a simple matching network.

Output Power adjustment

Power setting bits of Configuring word	RF output power	DC current consumption
11	0 dBm ±3dB	13.0 mA
10	-5 dBm ±3dB	10.5 mA
01	-10 dBm ±3dB	9.4 mA
00	-20 dBm ±3dB	8.8 mA

Conditions: VCC = 3.0V, VSS = 0V, TA = 27ºC, Load impedance = 400 ohm.

Table 15 RF output power setting for the TRF-2.4G.

Configuration Word Example

1 Channel, Freq.: 2410MHz, 1Mbps and Transmit mode:

Bit143	Bit142	Bit41	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit4	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0	**1**	**1**	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	**0**

Table 16 Configuration Example

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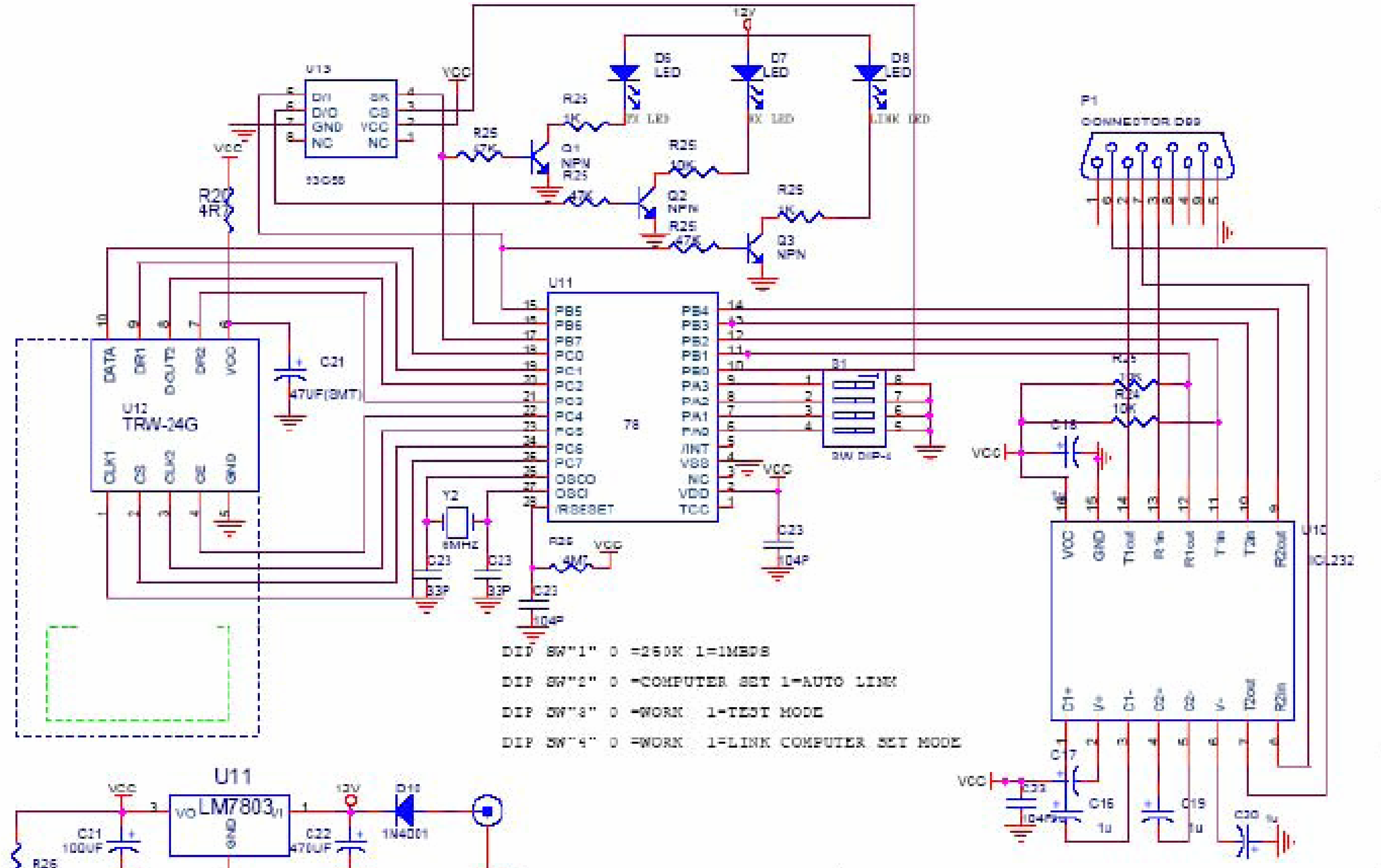

Title	Laipac Tech. Inc
Size A	2.4G RS232 Demo Board